

What is claimed is:

1. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of cross-over points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit is comprised of:
- 5 a MOS type transistor in which a gate electrode is connected to a scanning line and one of a source electrode and a drain electrode is connected to said signal line;
- 10 a MOS type analog amplifier circuit in which an input electrode is connected to another one of the source electrode and the drain electrode of said MOS type transistor, and an output electrode is connected to a pixel electrode; and
- 10 a voltage holding capacitor formed between an input electrode of said MOS type analog amplifier circuit and a voltage holding capacitor electrode.
2. An active matrix-type liquid crystal display device according to claim 1, wherein said MOS type transistor circuits are formed by thin film transistors.
3. An active matrix-type liquid crystal display device according to claim 1, wherein said liquid crystal display device include a liquid crystal material selected from the group consisting of a nematic liquid crystal or a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix
- 5 ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, and a monostable ferroelectric liquid crystal.

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4. A method of driving an active matrix-type liquid crystal display device according to claim 1, said method comprising the steps of:

storing data signals in the voltage holding capacitor through said MOS type transistor in a scanning line selection period; and

5 writing a signal corresponding to said stored data signal to a pixel electrode through said MOS type analog amplifier circuit in a scanning line selection period and a scanning line non-selection period.

5. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

85.3 5 ³⁰¹ an n-type MOS transistor having a gate electrode connected to a scanning line and a source electrode and a drain electrode, any one of which is connected to a signal line;

³⁰² a p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor and a source electrode and a drain electrode, one of which is connected to said scanning line, and
10 another one of the source electrode and the drain electrode connected to the pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and

a resistor connected between said pixel electrode and said voltage holding capacitor.

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6. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover

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points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to a scanning line and a source electrode and a drain electrode, any one of which is connected to a signal line;

a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor and a source electrode and a drain electrode, one of which is connected to said scanning line, and
10 another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and

a second p-type MOS transistor with a gate electrode connected to a voltage
15 adjustable power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

7. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to a scanning line and a source electrode and a drain electrode, one of which is connected to a signal line;

a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, a source electrode and a drain electrode, one of which is connected to said scanning line, and the source
10 electrode and the drain electrode, one of which is connected to a pixel electrode;

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a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and

15 a second p-type MOS transistor having a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode.

8. A liquid crystal display device wherein, in an active matrix type liquid crystal display device where pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor with a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and a source electrode and a drain electrode, another one of which is connected to said scanning line,

10 a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode, and

a second p-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode and a drain electrode connected to said pixel electrode.

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9. An active matrix-type liquid crystal display device according to claim 5, wherein the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

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10. An active matrix-type liquid crystal display device according to claim 5, wherein said resistance is formed by a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.

11. An active matrix-type liquid crystal display device according to claim 5, wherein a value of the resistance between the source and drain of said second p-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

12. An active matrix-type liquid crystal display device according to claim 5, wherein said MOS type transistor circuits are formed by integrating thin film transistors.

13. An active matrix-type liquid crystal display device according to claim 5, wherein the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, or a monostable ferroelectric liquid crystal.

14. A method of driving an active matrix-type liquid crystal display device according to claim 5, said method comprising the steps of:

supplying a voltage higher than a maximum voltage of said data signal to said voltage holding capacitor electrode;

5 storing data signals in said voltage holding capacitor through said n-type MOS transistor by means of a scanning pulse signal, and resetting said p-type MOS transistor or said first p-type MOS transistor by transferring the scanning pulse signal to said pixel

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electrode through said p-type MOS transistor or said first p-type MOS transistor, in a scanning line selection period; and

10 after completion of the scanning line selection period, writing signals corresponding to said stored data signals to pixel electrodes through said p-type MOS transistor or said first p-type MOS transistor.

15. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

an n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and a source electrode and a drain electrode, one of which is connected to said scanning line, and
10 another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said n-type MOS transistor and a voltage holding capacitor electrode; and

a resistor connected between said pixel electrode and said voltage holding capacitor
15 electrode.

16. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover

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points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first n-type MOS transistor having a gate electrode connected to the other of the source electrode and the drain electrode of said p-type MOS transistor, and a source electrode and a drain electrode, one of which is connected to said scanning line, and
10 another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode, and

a second n-type MOS transistor having a gate electrode connected to a voltage
15 adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

17. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and a source electrode and a drain electrode, one of which is connected to said scanning line, and

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10 another one of the source electrode and the drain electrode being connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode, and

a second n-type MOS transistor having a gate electrode connected to said voltage
15 holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode.

18. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line, a source electrode and a drain electrode, one of which is connected to a signal line;

a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode connected to said scanning line, and another one
10 of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode, and

a second n-type MOS transistor with a gate electrode and a source electrode
connected to said voltage holding capacitor electrode, and a drain electrode connected to
15 said pixel electrode.

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19. A liquid crystal display device according to claim 15, the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.
20. A liquid crystal display device according to claim 15, wherein said resistance is formed from a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.
21. A liquid crystal display device according to claim 16, wherein the value of a resistance between the source and the drain of said second n-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.
22. A liquid crystal display device according to claim 15, wherein said MOS type transistor circuits are formed by integrating thin film transistors.
23. A liquid crystal display device according to claim 15, wherein the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, and a monostable ferroelectric liquid crystal.
24. A method of driving an active matrix-type liquid crystal display device according to claim 15, said method comprising the steps of:

supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

5 storing a data signal in said voltage holding capacitor through said p-type MOS transistor by means of a scanning pulse signal, and resetting said n-type MOS transistor or said first n-type MOS transistor by transferring the scanning pulse signal to said pixel electrode through said n-type MOS transistor or said first n-type MOS transistor in a scanning line selection period; and

10 after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to pixel electrode through said n-type MOS transistor or said first n-type MOS transistor.

25. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to an Nth (where N is an integer of two or more) scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and a source
10 electrode and a drain electrode, one of which is connected to an (N-1)th scanning line, and another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said p-type MOS transistor and a voltage holding capacitor electrode; and

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15 a resistor connected between said pixel electrode and said voltage holding capacitor electrode.

26. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to an Nth scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and one of a source electrode and a drain electrode connected to an (N-1)th scanning line, and the
10 other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and

a second p-type MOS transistor having a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding
15 capacitor electrode, and a drain electrode connected to said pixel electrode.

27. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to an Nth scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

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MOS transistor and a voltage holding capacitor electrode; and

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transistor circuit comprises:

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MOS transistor and a voltage holding capacitor electrode; and

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29. A liquid crystal display device according to claim 25, wherein the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

30. A liquid crystal display device according to claim 25, wherein said resistance is formed from a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.

31. A liquid crystal display device according to claim 25, wherein the value of the resistance between the source and drain of said second p-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

32. A liquid crystal display device according to claim 25, wherein said MOS type transistor circuits are formed by integrating thin film transistors.

33. A liquid crystal display device according to claim 25, the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, or a monostable ferroelectric liquid crystal.

34. A method of driving a liquid crystal display device according to claim 25 comprising the steps of:

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5 in a scanning line selection period of a previous line, resetting said p-type MOS transistor or said first p-type MOS transistor by transferring the scanning pulse signal of the previous line to said pixel electrode through said p-type MOS transistor or said first p-type MOS transistor, and

35. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

a n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode connected to an (N-1)th scanning line, and another one of the source electrode and the drain electrode connected to a pixel electrode,

15 a resistor connected between said pixel electrode and said voltage holding capacitor electrode.

5 a p-type MOS transistor having a gate electrode connected to an Nth (where N is an integer of two or more) scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode, and

37. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover

points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to an Nth (where N is an integer of two or more) scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode connected to an (N-1)th scanning line, and another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and

15 a second n-type MOS transistor having a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode.

38. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to an Nth (where N is an integer of two or more) scanning line, and one of a source electrode and a drain electrode connected to a signal line;

a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a

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- 10 source electrode and a drain electrode connected to an (N-1)th scanning line, and another
one of the source electrode and the drain electrode connected to a pixel electrode;
a voltage holding capacitor formed between the gate electrode of said first n-type
MOS transistor and a voltage holding capacitor electrode; and
a second n-type MOS transistor with a gate electrode and a source electrode
15 connected to said voltage holding capacitor electrode, and a drain electrode connected to
said pixel electrode.

39. A liquid crystal display device according to claim 35, wherein the value of said
resistance is set to less than or equal to the value of a resistance component which
determines a response time constant of the liquid crystal.

40. A liquid crystal display device according to claim 35, said resistance is formed
from a semiconductor thin film, or a semiconductor thin film which has been doped with
impurities.

41. A liquid crystal display device according to claim 36, the value of a resistance
between the source and drain of said second n-type MOS transistor is set to less than or
equal to the value of a resistance component which determines a response time constant
of the liquid crystal.

42. A liquid crystal display device according to claim 35, said MOS type transistor
circuits are formed by integrating thin film transistors.

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43. A liquid crystal display device according to claim 35, the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, or a monostable ferroelectric liquid crystal.

44. A method of driving a liquid crystal display device according to claim 35, said method comprising the steps of:

supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

5 in a scanning line selection period of the previous line, resetting said n-type MOS transistor or said first n-type MOS transistor by transferring the scanning pulse signal of the previous line to said pixel electrode through said n-type MOS transistor or said first n-type MOS transistor;

10 in a scanning line selection period, storing a data signal in said voltage holding capacitor through said p-type MOS transistor by means of a scanning pulse signal, and writing a signal corresponding to said stored data signal to a pixel electrode through said n-type MOS transistor or said first n-type MOS transistor, and

15 after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said n-type MOS transistor or said first n-type MOS transistor.

45. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of

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intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and one of a source electrode and a drain electrode connected to a reset electrode, and another one of
10 the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said p-type MOS transistor and a voltage holding capacitor electrode; and

a resistor connected between said pixel electrode and said voltage holding capacitor electrode.

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46. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and one of a source electrode and a drain electrode connected to a reset electrode, and the other of the
10 source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode, and

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15 a second p-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

47. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 an n-type MOS transistor with a gate electrode connected to a scanning line, and one of a source electrode and a drain electrode connected to a signal line;

10 a first p-type MOS transistor with a gate electrode connected to the other of the source electrode and the drain electrode of said n-type MOS transistor, and one of a source electrode and a drain electrode connected to a reset electrode, and the other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and

15 a second p-type MOS transistor with a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode.

48. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

- 5 an n-type MOS transistor with a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;
- a first p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS transistor, and one of a source electrode and a drain electrode connected to a reset electrode, and the other of the
- 10 source electrode and the drain electrode connected to a pixel electrode;
- a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and
- a second p-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to
- 15 said pixel electrode.

49. A liquid crystal display device according to claim 45, the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

50. A liquid crystal display device according to claim 45, said resistance is formed from a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.

51. A liquid crystal display device according to claim 46, the value of a resistance between the source and drain of said second p-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

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52. A liquid crystal display device according to claim 45, said MOS type transistor circuits are formed by integrating thin film transistors.

53. A liquid crystal display device according to claim 45, the liquid crystal material is selected from a group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, or a monostable ferroelectric liquid crystal.

54. A method of driving a liquid crystal display device according to claim 35 comprising the steps of:

supplying a voltage higher than a maximum voltage of said data signal to said voltage holding capacitor electrode;

5 in a previous time prior to the scanning line selection period, resetting said p-type MOS transistor or said first p-type MOS transistor by transferring a reset signal to said pixel electrode through said p-type MOS transistor or said first p-type MOS transistor;

10 in a scanning line selection period, storing a data signal in said voltage holding capacitor through said n-type MOS transistor by means of a scanning pulse signal, and writing a signal corresponding to said stored data signal to a pixel electrode through said p-type MOS transistor or said first p-type MOS transistor; and

after completion of the scanning line selection period, writing the signals corresponding to said stored data signal to the pixel electrode through said p-type MOS transistor or said first p-type MOS transistor.

55. A method of driving a liquid crystal display device according to claim 45, said method comprises the steps of:

supplying a voltage higher than a maximum voltage of said data signal to said voltage holding capacitor electrode;

5 in a scanning line selection period, storing a data signal in said voltage holding capacitor through said n-type MOS transistor by means of a scanning pulse signal, and resetting said p-type MOS transistor or said first p-type MOS transistor by transferring a reset signal to said pixel electrode through said p-type MOS transistor or said first p-type MOS transistor; and

10 after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said p-type MOS transistor or said first p-type MOS transistor.

56. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line and a source electrode and a drain electrode, one of which is connected to a signal line;

an n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and the other
10 of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said n-type MOS transistor and a voltage holding capacitor electrode, and

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a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and the other

a second n-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

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a p-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line,

10 a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode connected to a reset electrode, and the other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and

15 a second n-type MOS transistor having a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode.

59. An active matrix type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a p-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

10 a first n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and

15 a second n-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

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60. A liquid crystal display device according to claim 56, wherein the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

61. A liquid crystal display device according to claim 56, wherein said resistance is formed from a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.

62. A liquid crystal display device according to claim 57, wherein the value of a source-drain resistance of said second n-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

63. A liquid crystal display device according to claim 56, wherein said MOS type transistor circuits are formed by integrating thin film transistors.

64. A liquid crystal display device according to claim 56, wherein the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, and a monostable ferroelectric liquid crystal.

65. A method of driving a liquid crystal display device according to claim 56, said method comprising the steps of:

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supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

5 at a time prior to a scanning line selection period, resetting said n-type MOS transistor or said first n-type MOS transistor by transferring a reset signal to said pixel electrode through said n-type MOS transistor or said first n-type MOS transistor;

in a scanning line selection period, storing a data signal in said voltage holding capacitor through said n-type MOS transistor by means of a scanning pulse signal, and

10 writing a signal corresponding to said stored data signal to a pixel electrode through said n-type MOS transistor or said first n-type MOS transistor, and

after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to the pixel electrode through said n-type MOS transistor or said first n-type MOS transistor.

15 66. A method of driving a liquid crystal display device according to claim 56, said method comprising the steps of:

supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

5 in a scanning line selection period, storing a data signal in said voltage holding capacitor through said p-type MOS transistor by means of a scanning pulse signal,

resetting said n-type MOS transistor or said first n-type MOS transistor by transferring a reset signal to said pixel electrode through said n-type MOS transistor or said first n-type MOS transistor; and

10 after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said n-type MOS transistor or said first n-type MOS transistor.

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67. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first n-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

10 a second n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first n-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and the other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said second n-type MOS transistor and a voltage holding capacitor electrode; and

a resistor connected between said pixel electrode and said voltage holding capacitor electrode.

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68. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first n-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a second n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first n-type MOS transistor, and one

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of a source electrode and a drain electrode being connected to a reset electrode, and the
10 other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said second n-type
MOS transistor and a voltage holding capacitor electrode; and

a third n-type MOS transistor with a gate electrode connected to a voltage adjustable
bias power supply line, a source electrode connected to said voltage holding capacitor
15 electrode, and a drain electrode connected to said pixel electrode.

69. An active matrix-type liquid crystal display device in which pixel electrodes are
driven by MOS type transistor circuits respectively disposed in the vicinity of
intersection point of a plurality of scanning lines and a plurality of signal lines, said
MOS type transistor circuit comprises:

5 a first n-type MOS transistor having a gate electrode connected to a scanning line, and
a source electrode and a drain electrode, one of which is connected to a signal line,

a second n-type MOS transistor having a gate electrode connected to another one of
the source electrode and the drain electrode of said first n-type MOS transistor, and one
of a source electrode and a drain electrode being connected to a reset electrode, and
10 another one of the source electrode and the drain electrode connected to a pixel
electrode;

a voltage holding capacitor formed between the gate electrode of said second n-type
MOS transistor and a voltage holding capacitor electrode; and

a third n-type MOS transistor having a gate electrode connected to said voltage
15 holding capacitor electrode, a source electrode connected to a voltage adjustable bias
power supply line, and a drain electrode connected to said pixel electrode.

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70. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first n-type MOS transistor having a gate electrode connected to a scanning line, and a source electrode and a drain electrode, one of which is connected to a signal line;

a second n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first n-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and

10 another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said second n-type MOS transistor and a voltage holding capacitor electrode; and

15 a third n-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode.

71. A liquid crystal display device according to claim 67, the value of said resistance is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

72. A liquid crystal display device according to claim 67, wherein said resistance is formed from a semiconductor thin film, or a semiconductor thin film which has been doped with impurities.

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73. A liquid crystal display device according to claim 68, wherein the value of a resistance between the source and drain of said third n-type MOS transistor is set to less than or equal to the value of a resistance component which determines a response time constant of the liquid crystal.

74. A liquid crystal display device according to claim 67, said MOS type transistor circuits are formed by integrating thin film transistors.

75. A liquid crystal display device according to claim 67, the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal, or a monostable ferroelectric liquid crystal.

76. A method of driving a liquid crystal display device according to claim 67, said method comprising the steps of:

supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

at a time prior to a scanning line selection period, resetting said second n-type MOS transistor by transferring a reset signal to said pixel electrode through said second n-type MOS transistor;

in a scanning line selection period, storing a data signal in said voltage holding capacitor through said first n-type MOS transistor by means of a scanning pulse signal,

writing a signal corresponding to said stored data signal to a pixel electrode through said second n-type MOS transistor, and

after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said second n-type MOS transistor.

77. A method of driving a liquid crystal display device according to claim 67, said method comprising the steps of:

supplying a voltage lower than a minimum voltage of said data signal to said voltage holding capacitor electrode;

5 in a scanning line selection period, storing a data signal in said voltage holding capacitor through said first n-type MOS transistor by means of a scanning pulse signal, and resetting said second n-type MOS transistor by transferring a reset signal to said pixel electrode through said second n-type MOS transistor;

10 and after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said second n-type MOS transistor.

78. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first p-type MOS transistor having a gate electrode connected to a scanning line, and one of a source electrode and a drain electrode connected to a signal line;

a second p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and

10 another one of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and

15 a resistor connected between said pixel electrode and said voltage holding capacitor electrode.

79. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of intersection point of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first p-type MOS transistor with a gate electrode connected to a scanning line, and a source electrode and a drain electrode connected to a signal line;

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a second p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and the
10 other of the source electrode and the drain electrode connected to a pixel electrode;

a voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and

a third p-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacity
15 electrode, and a drain electrode connected to said pixel electrode.

80. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover

5 a first p-type MOS transistor having a gate electrode connected to a scanning line, and
a source electrode and a drain electrode, one of which is connected to a signal line;

10 another one of the source electrode and the drain electrode connected to a pixel
electrode;

a voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and

15 a third p-type MOS transistor with a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable bias power supply line, and a drain electrode connected to said pixel electrode.

81. An active matrix-type liquid crystal display device in which pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines and a plurality of signal lines, said MOS type transistor circuit comprises:

5 a first p-type MOS transistor having a gate electrode connected to a scanning line, and
a source electrode and a drain electrode, one of which is connected to a signal line;

a second p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said first p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and

10 another one of the source electrode and the drain electrode connected to a pixel
electrode;

a voltage holding capacitor formed between the gate electrode of said second p-type
MOS transistor and a voltage holding capacitor electrode; and

a third p-type MOS transistor having a gate electrode and a source electrode
15 connected to said voltage holding capacitor electrode, and a drain electrode connected to
said pixel electrode.

82. A liquid crystal display device according to claim 78, wherein the value of said
resistance is set to less than or equal to the value of a resistance component which
determines a response time constant of the liquid crystal.

83. A liquid crystal display device according to claim 78, wherein said resistance is
formed from a semiconductor thin film or a semiconductor thin film which has been
doped with impurities.

84. A liquid crystal display device according to claim 79, wherein the value of a
source-drain resistance of said third p-type MOS transistor is set to less than or equal to
the value of a resistance component which determines a response time constant of the
liquid crystal.

85. A liquid crystal display device according to claim 78, wherein said MOS type
transistor circuits are formed by integrating thin film transistors.

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86. A liquid crystal display device according to claim 78, wherein the liquid crystal material is selected from the group consisting of a nematic liquid crystal, a ferroelectric liquid crystal, an antiferroelectric liquid crystal, a thresholdless antiferroelectric liquid crystal, a distorted helix ferroelectric liquid crystal, a twisted ferroelectric liquid crystal,
5 and a monostable ferroelectric liquid crystal.

87. A method of driving a liquid crystal display device according to claim 78, said method of driving comprising the steps of:

supplying a voltage higher than a maximum voltage of said data signal to said voltage holding capacitor electrode;

5 at a time prior to a scanning line selection period, resetting said second p-type MOS transistor by transferring a reset signal to said pixel electrode through said second p-type MOS transistor;

in a scanning line selection period, storing a data signal in said voltage holding capacitor through said first p-type MOS transistor by means of a scanning pulse signal,
10 and writing a signal corresponding to said stored data signal to a pixel electrode through said second p-type MOS transistor, and

after completion of the scanning line selection period, writing a signal corresponding to said stored data signal to a pixel electrode through said second p-type MOS transistor.

88. A method of driving a liquid crystal display device according to claim 78, said method comprising the steps of:

supplying a voltage higher than a maximum voltage of said data signal to said voltage holding capacitor electrode;

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after completion of the scanning line selection period, writing a signal corresponding
10 to said stored data signal to a pixel electrode through said second p-type MOS transistor.

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